Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2026

Third Semester

Electrical and Electronics Engineering

EE3302 – DIGITAL LOGIC CIRCUITS

Regulations - 2021

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A(ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	Questions	BTL	CO	Marks
1.	Find the decimal number $(126)_{10}$ into octal number.	L1	1	2
2.	Demonstrate the given Boolean expression $y = \overline{ABC} + \overline{A}B\overline{C} + A\overline{BC} + AB\overline{C}$	L2	1	2
3.	Relate the simplified function f in POS form.	L2	2	2
4.	Label the 1:8 De- Mux circuit.	L1	2	2
5.	The present state Q_n of edge triggered JK flip-flop, Q_n=0. Identify the next stage Q_{n+1} if J=1 and K=0.	L2	3	2
6.	Compare synchronous and asynchronous type sequential circuits.	L2	3	2
7.	Mention when an asynchronous sequential circuit is said to be hazard free.	L1	4	2
8.	Outline the meaning of critical and non-critical races in asynchronous circuits.	L2	4	2
9.	Show the syntax of Verilog programming module.	L1	5	2
10.	Recall the use of component declaration.	L1	5	2

A	B	C	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
0	0	1	0
1	1	0	1
	1	1	0

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			Questions	BLT	CO	Marks
11.	a	i	Simplify the given function using QM Method $F(w,x,y,z) = \sum m\,(1,3,7,11,15) + \sum d\,(0,2,5).$	L4	1	10
		ii	Function $A + BC' + ABD' + ABCD$ to minterm and maxterm.	L4	1	6
			Or			
	b	i	Draw the circuit diagram of TTL and Survey the operation.	L4	1	8
		ii	Contrast the ECL operation with its neat diagram.	L4	1	8
12.	a	i	Reduce the expression $f = \sum m\,(0,1,2,3,5,7,8,9,10,12,13)$ using k-map and implement the real minimal expression in universal logic.	L3	2	8
		ii	Express the function $Y = A + \overline{B}C$ in canonical SOP and canonical POS form.	L3	2	8
			Or			
	b	i	Develop a 4 bit Binary to Gray code converter.	L3	2	8

		ii	Build a combinational logic circuit using 4 to 16-line decoder to implement function $F = \sum m(2,3,9,11)$	L3	2	8
13.	a		Examine the SR flip-flop by providing the state table, logic circuit and characteristic equation. Also show how an SR flip-flop can be converted into a D flip-flop.	L4	3	16
			Or			
	b		Draw the logic diagram and analyze the truth table for mod-10 counter using flip-flops.	L4	3	16
14.	a		Evaluate an asynchronous sequential circuit with two inputs X & Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X.	L5	4	16
			Or			
	b		Conclude the features and characteristics of PLA and CPLD devices.	L5	4	16
15.	a	i	Write the VHDL code for a logical gate which gives high output only when both the inputs are high.	L2	5	8
		ii	Explain functions and subprograms with suitable examples	L2	5	8
			Or			
	b	i	Draw the logic diagram and write Gate level description in Verilog HDL code for Full Adder and Demultiplexer.	L2	5	16